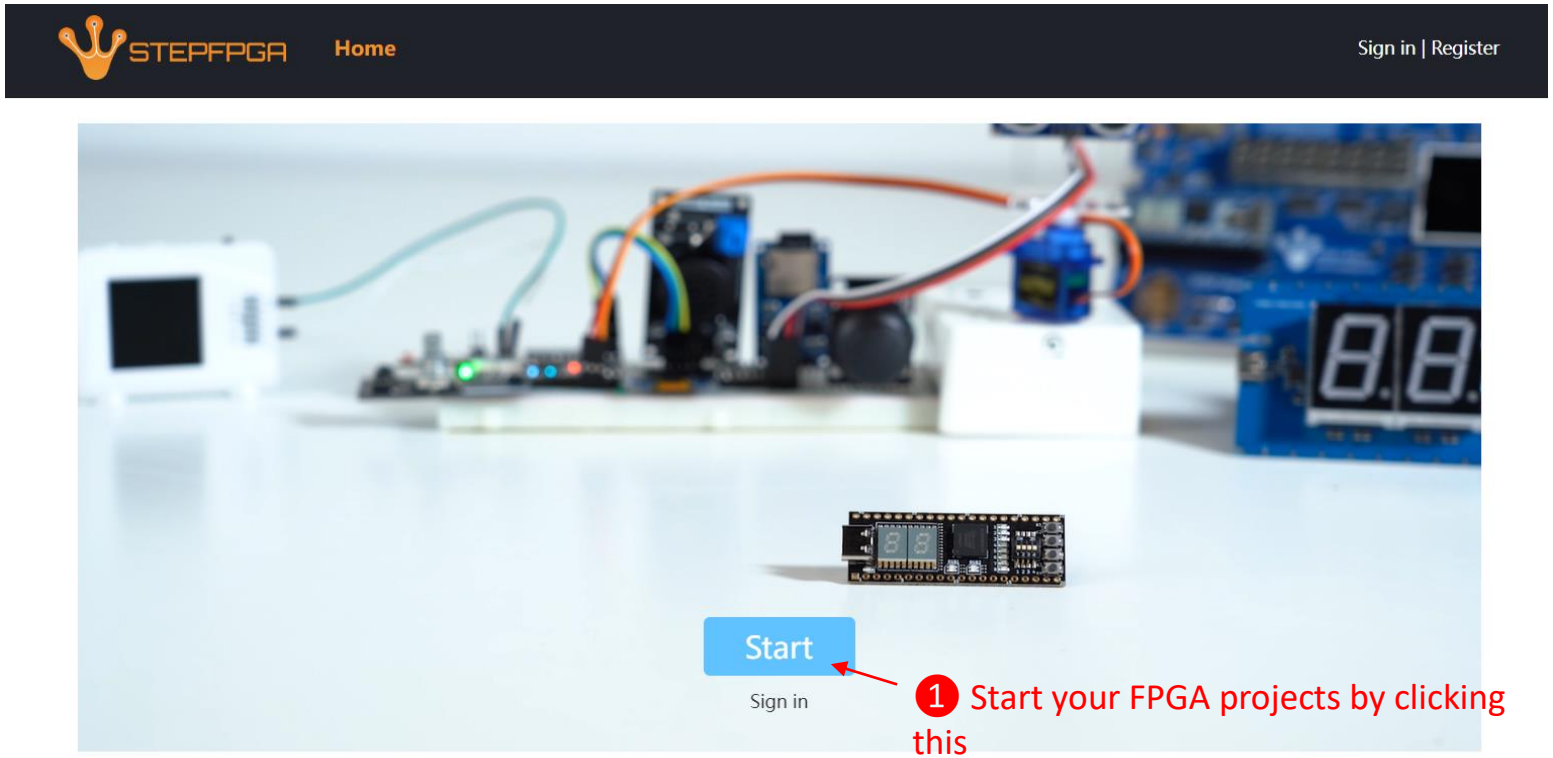
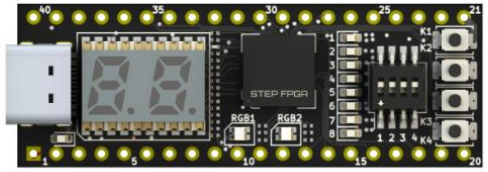
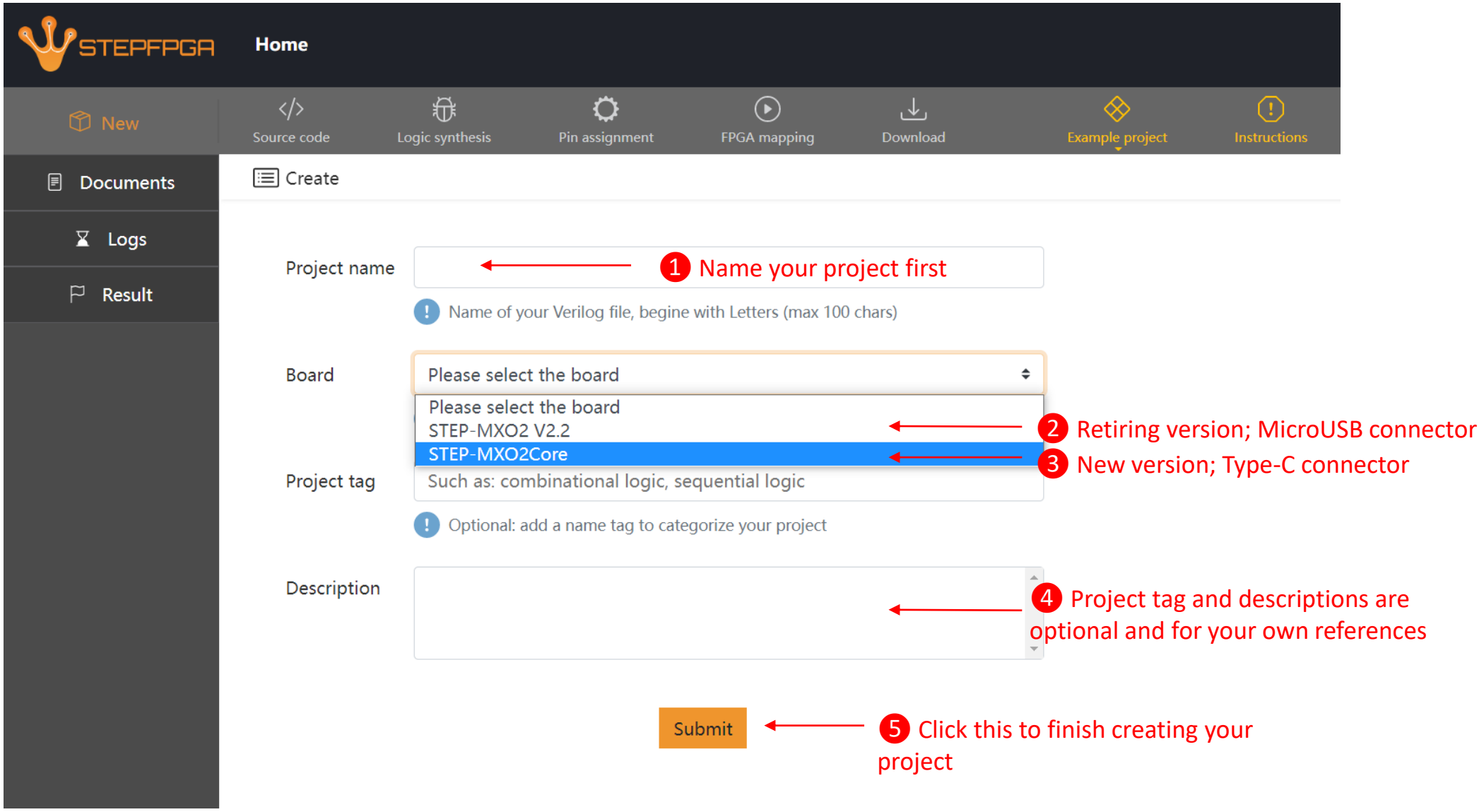
Start your FPGA project on WebIDE (stepfpga.eimtechnology.com)



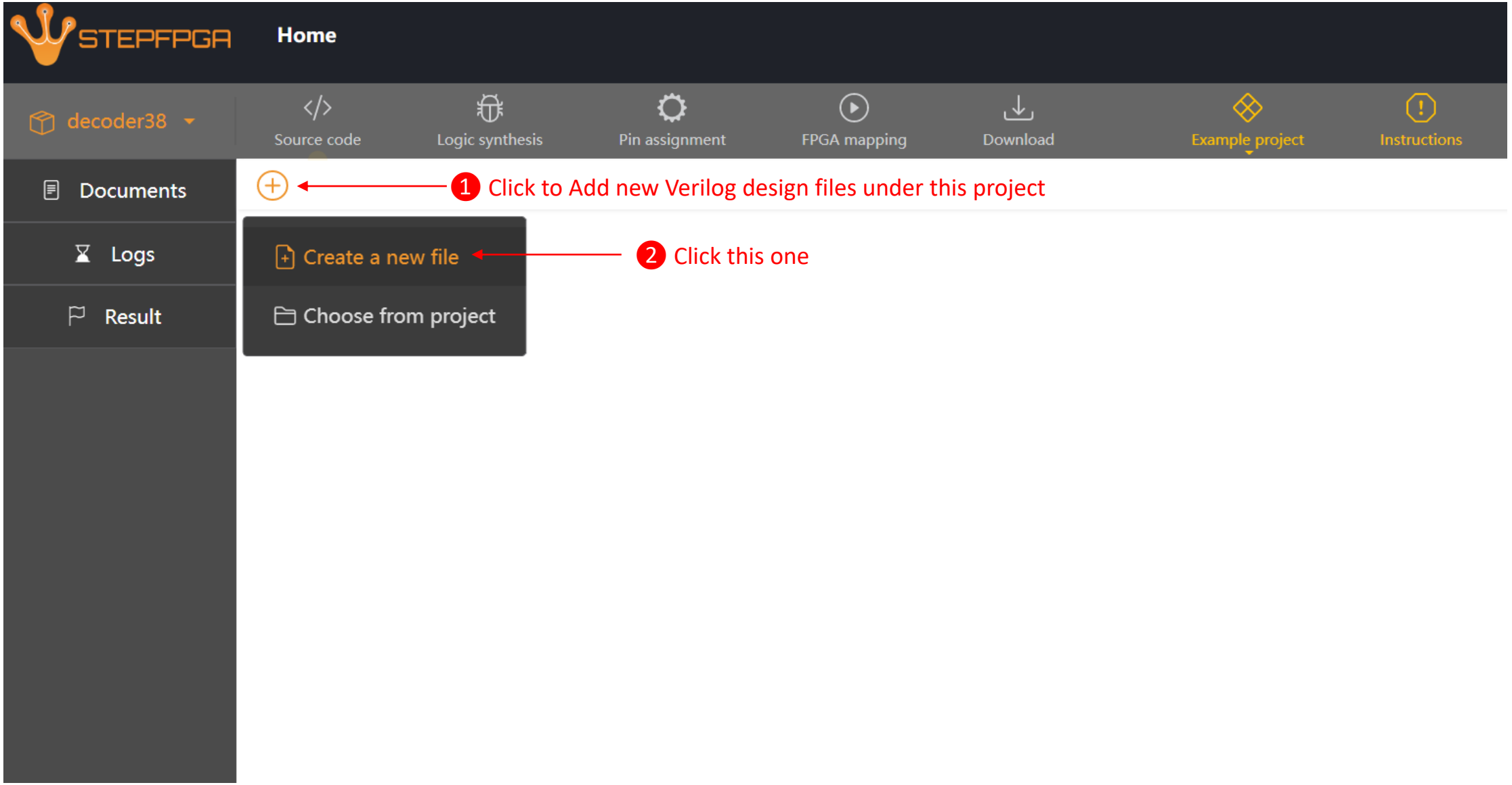


Design, Develop, and Share your FPGA source code

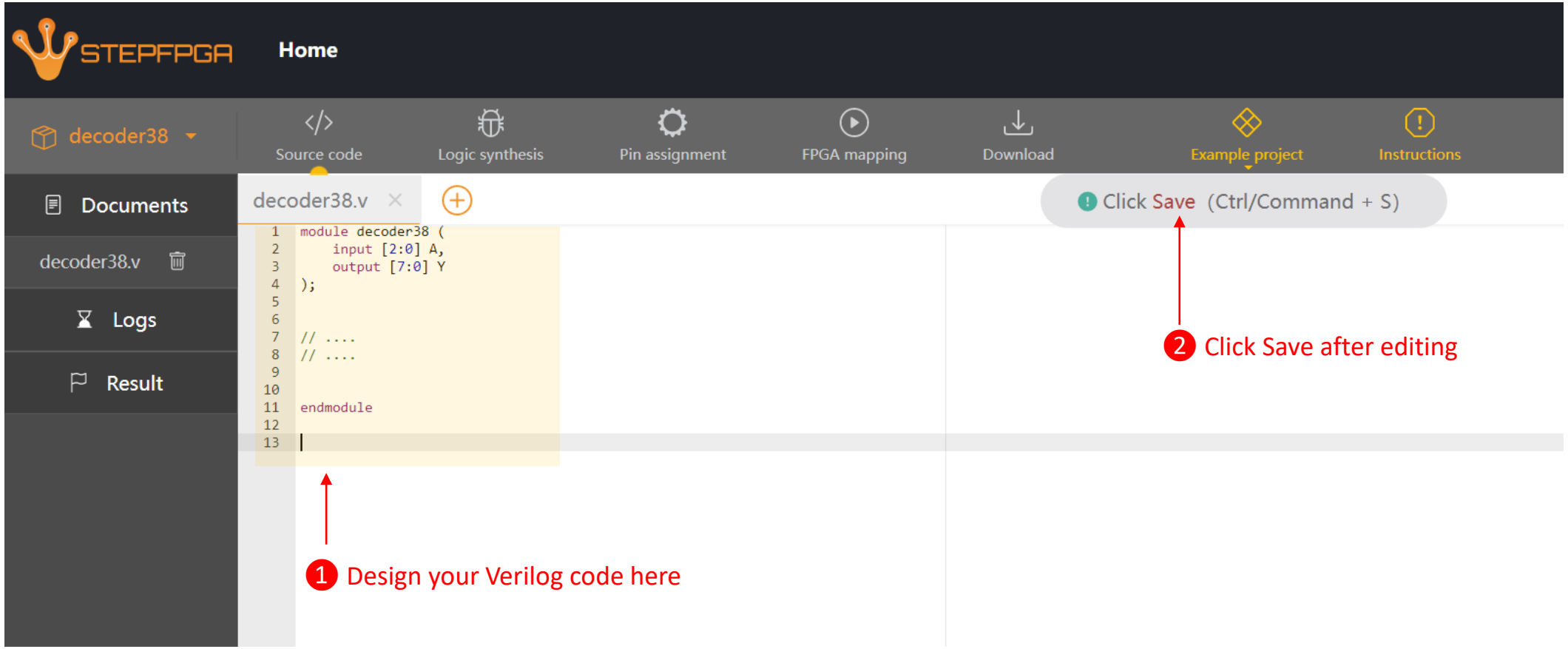
Create a project



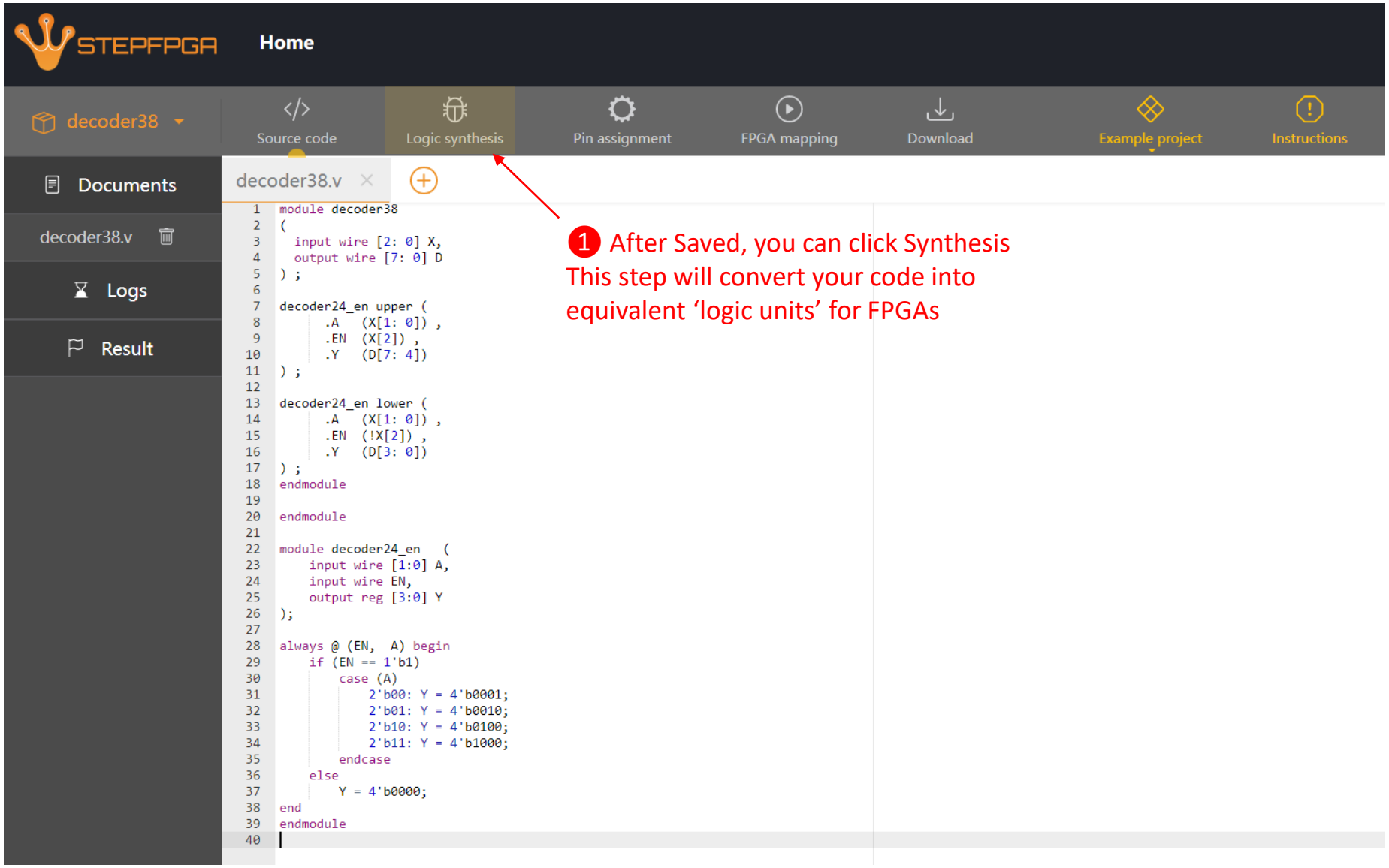
Create a Verilog design file



Code Editing Interface

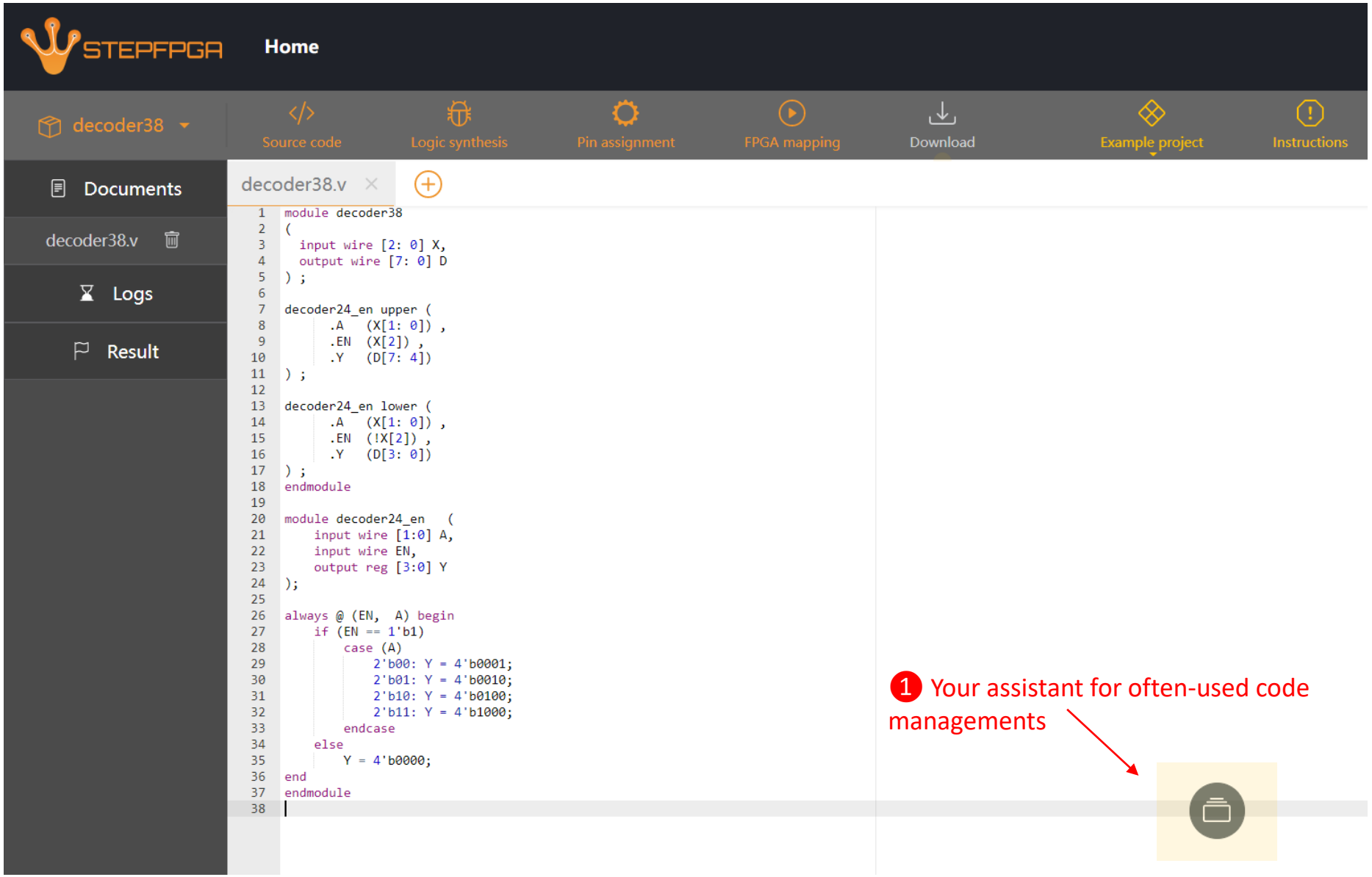


Continue to Logic Synthesis

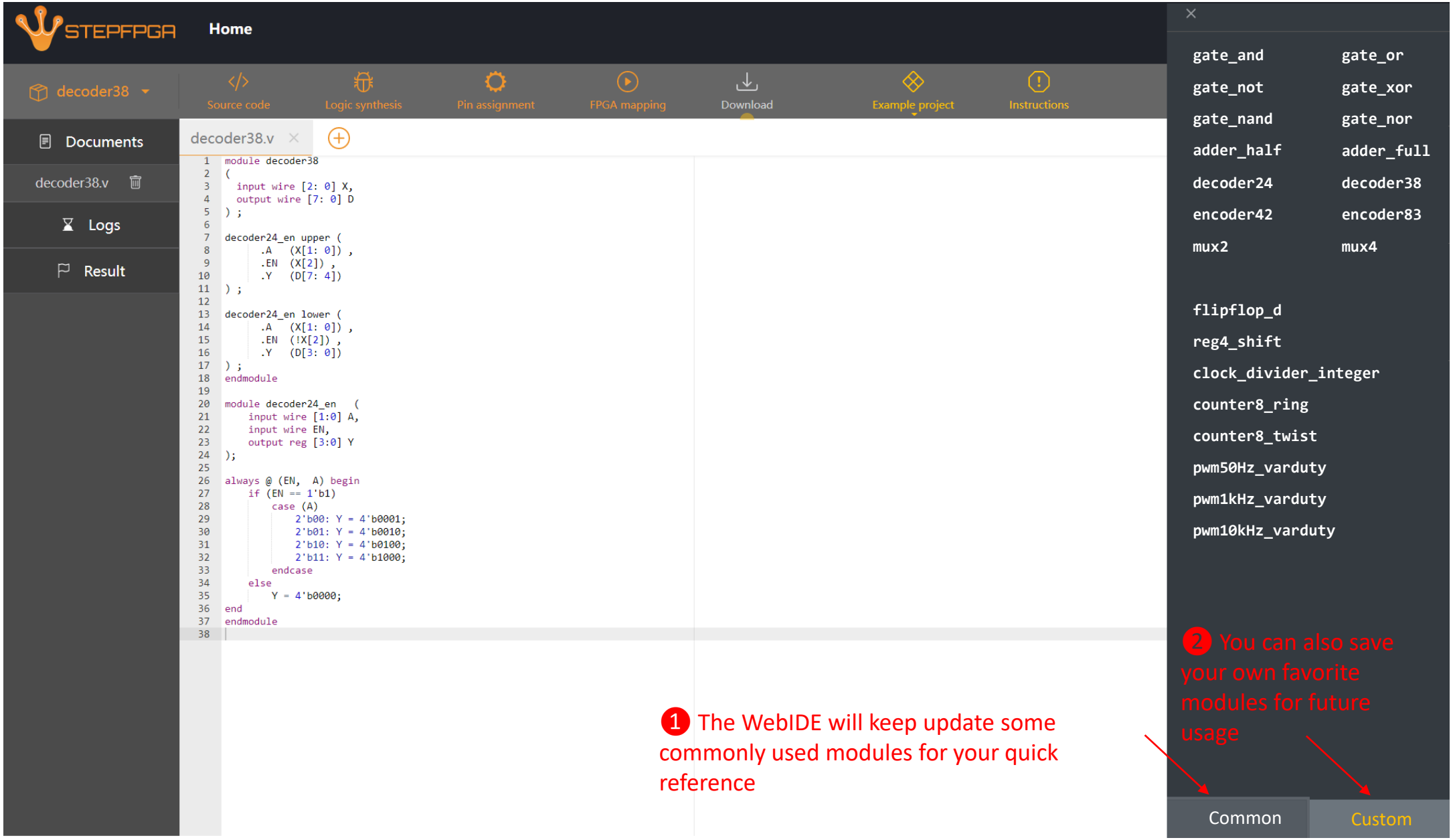



```
module decoder38
(
  input wire [2: 0] X,
  output wire [7: 0] D
) ;

decoder24_en upper (
      .A   (X[1: 0]) ,
      .EN  (X[2]) ,
      .Y   (D[7: 4])
) ;

decoder24_en lower (
      .A   (X[1: 0]) ,
      .EN  (!X[2]) ,
      .Y   (D[3: 0])
) ;
endmodule

endmodule

module decoder24_en   (
    input wire [1:0] A,
    input wire EN,
    output reg [3:0] Y
);

always @ (EN,  A) begin
    if (EN == 1'b1)
        case (A)
            2'b00: Y = 4'b0001;
            2'b01: Y = 4'b0010;
            2'b10: Y = 4'b0100;
            2'b11: Y = 4'b1000;
        endcase
    else
        Y = 4'b0000;
end
endmodule
```

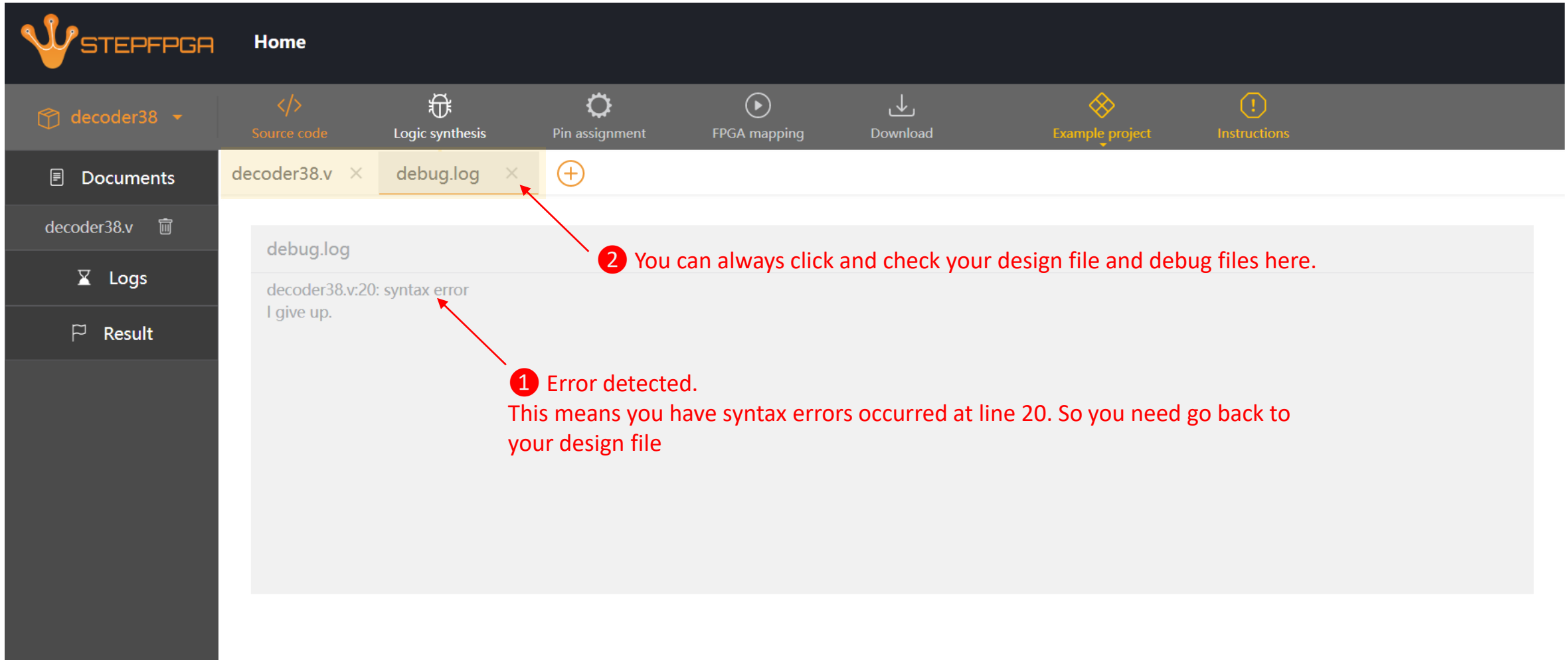
A tip for quick design



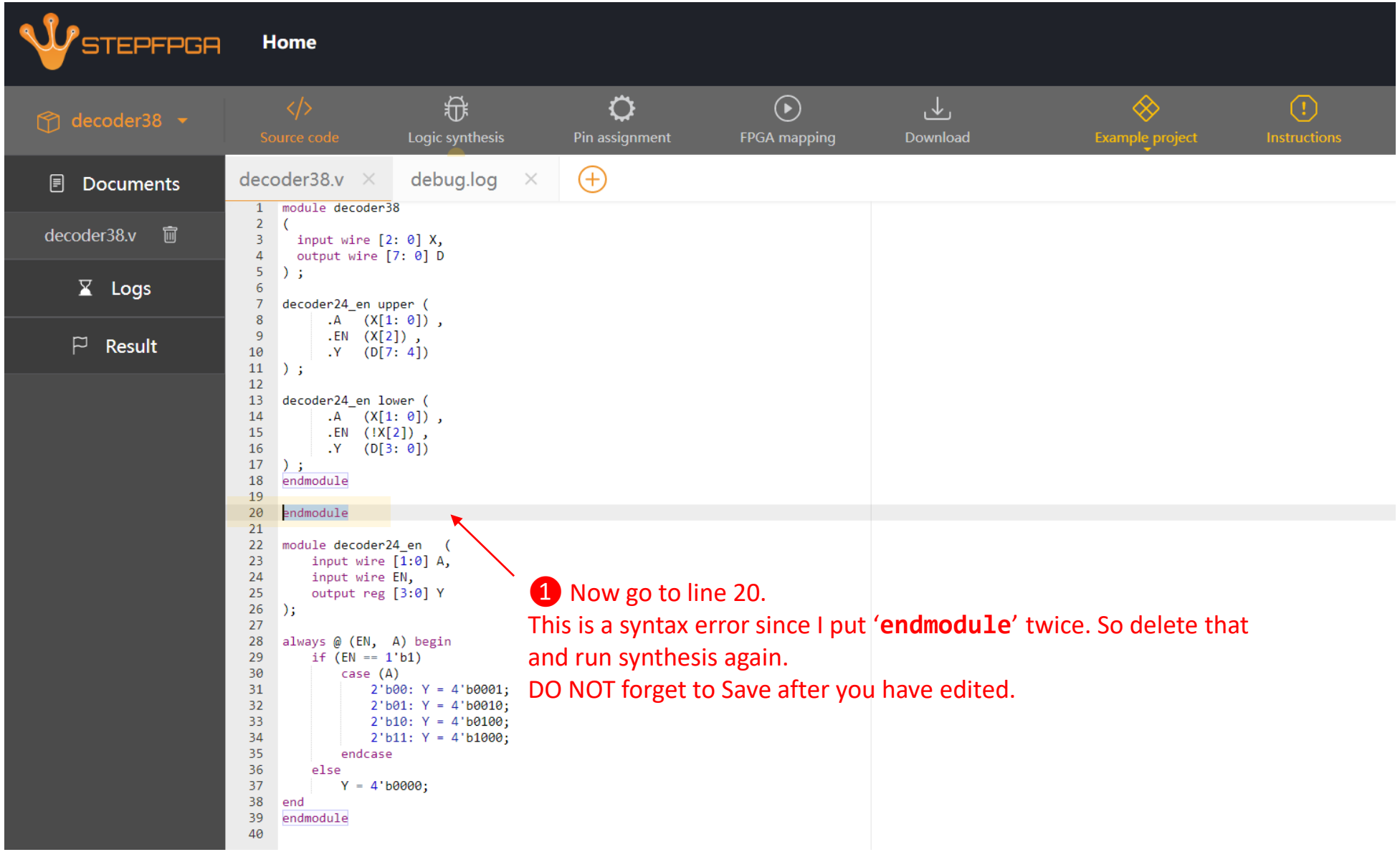
Manage your own workpieces



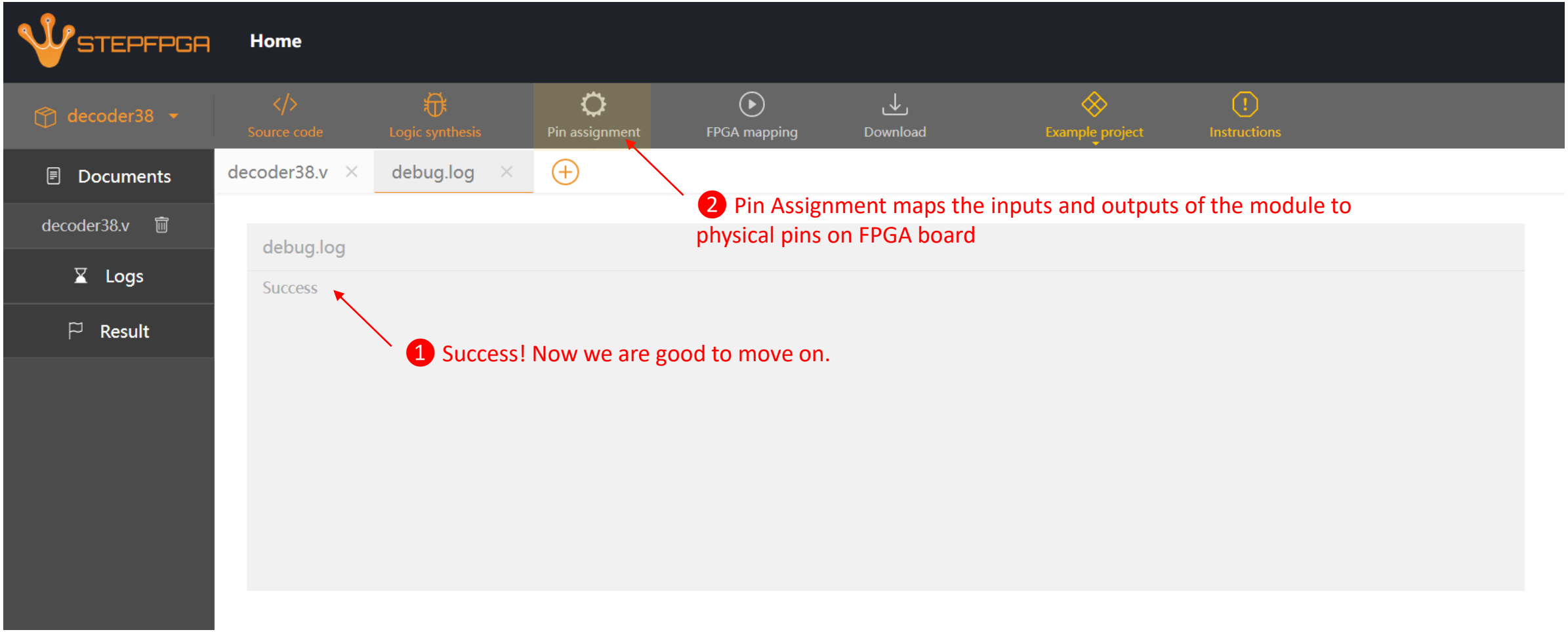
Showing debug information of your code



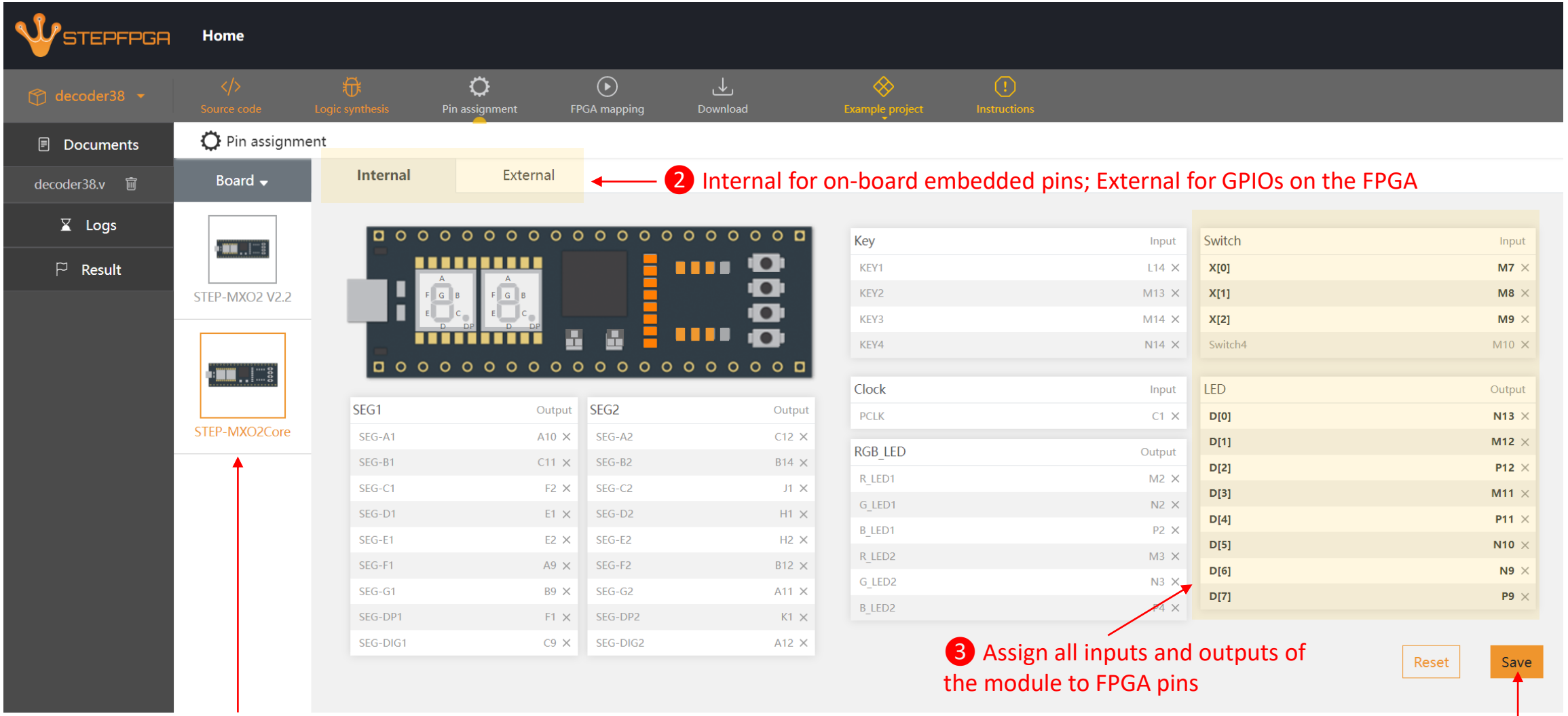
Trace your error



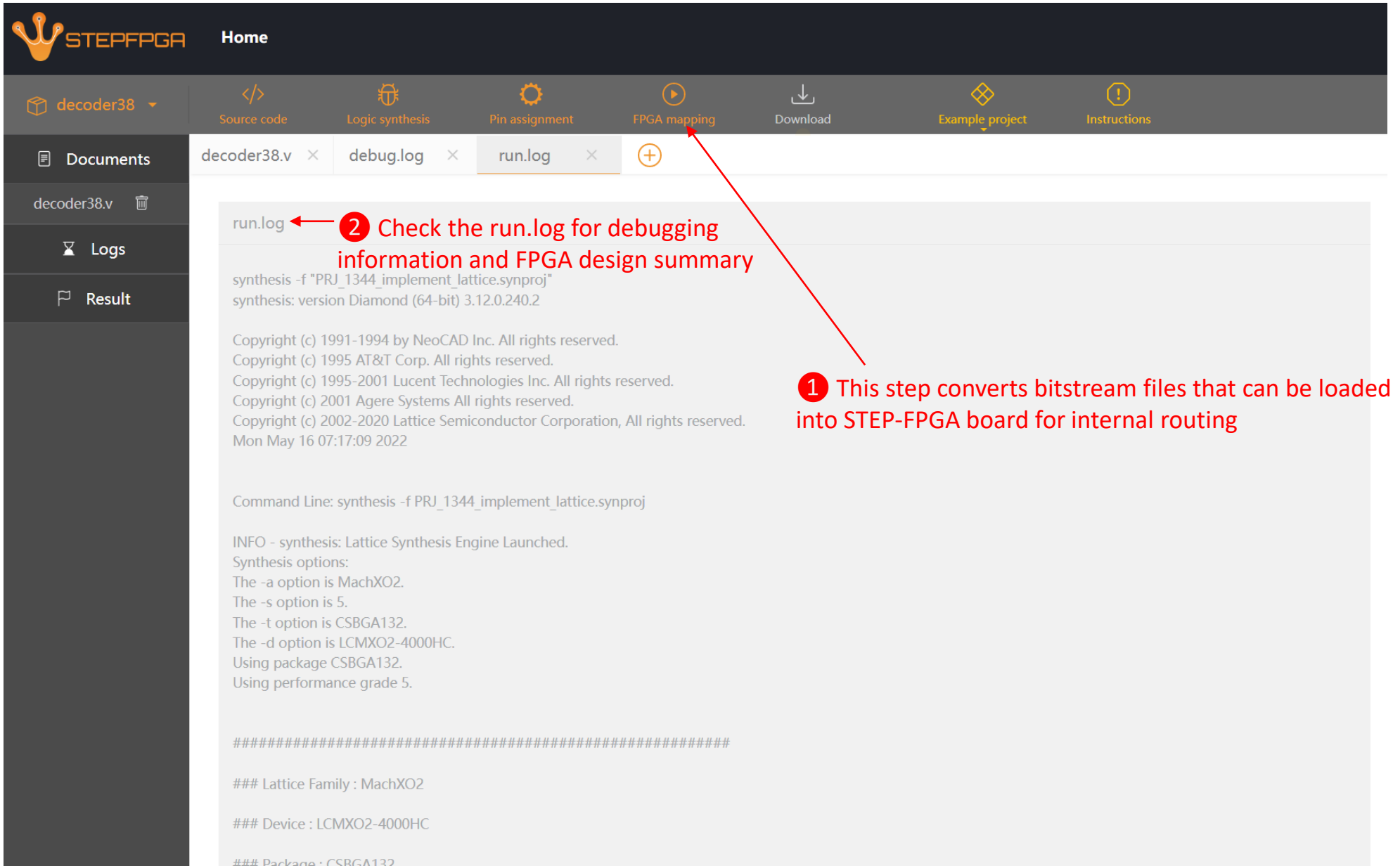
Continue to Pin Assignment



Visualize the Pin Assignment with one glimpse



Check for FPGA internal routing summary information



Burn the code into STEP FPGA board